Claim 2, line 3, please delete the word "substantially".

9. A system for testing logic semiconductor integrated circuits, comprising:

a circuit analysis tool; and

means for automatically:

applying to the circuit analysis tool generalized failure data;

obtaining from the circuit analysis tool localized probable defect data and circuit models describing logical operations of the integrated circuits;

representing the localized probable defect data in a standard format; and

storing the localized probable defect data on a database server accessible to multiple client machines.

REMARKS

The Office Action of February 3, 2000 has been carefully considered. In response thereto, the claims have been amended as set forth above. Withdrawal of the rejection and allowance of the present application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-8 were rejected as being anticipated by Lindsay, and claim 9 was rejected as being unpatentable over the same. Claims 1 and 4-6 were rejected as being unpatentable over Burdick, and claim 9 was rejected as being unpatentable over the same. Finally, claims 2, 3, 7 and 8 were rejected as being unpatentable over Burdick in view of Lindsay.

Claims 1 and 9 have been amended to more clearly distinguish over the cited references. Reconsideration is respectfully requested.

In particular, claims 1 and 9 have been amended to make clear that the present invention pertains to *logic* integrated circuits as opposed to memory ICs.

The regularized array structure of memory ICs makes them very readily testable. As described in the BACKGROUND portion of the specification, however, failure analysis of logic part is much more problematic. The present invention provides a novel, valuable technique for testing logic integrated circuits.

Lindsay relates to testing of memory devices and is representative of techniques described in the BACKGROUND section. Lindsay does not pertain to the testing of logic integrated circuits.

Burdick describes a technique for pretesting ICs for assembly into Multi-Chip Modules (MCMs) to make available "Fabrication-Ready" die for use in the fabrication of MCMs, reducing rework costs in the case of device failure. Frames of die are placed in a standard probe station and tested using conventional test systems and interface hardware. A full component test duplicating the manufacturer's test, is not intended nor required. Visual inspection is also performed. Visual test may include gross incoming visual inspection and more thorough, post electrical test, visual inspection. The IC pretest method is described as significantly increasing MCM yield while keeping the overall MCM cost at a minimum.

Although Burdick describes the use of electrical and visual tests in conjunction with one another, there is absolutely no description in Burdick of converting generalized electrical failure data to localized probably defect data and of correlating first (i.e., electrical) and second (i.e., visual) localized probably defect data as claimed. This conclusion is further supported by recognizing that Burdick is not at all concerned with failure analysis but only in evaluating the fabrication-readiness of dies for purposes of MCM manufacture. Failure analysis, which is a primary use of the present invention, is

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the problem of the device manufacturer and not the MCM manufacturer. Hence, although the various passages cited in Burdick do address various aspects of electrical testing and visual testing used in conjunction with one another, they in no way describe or suggest the essential steps of the present invention.

Withdrawal of the rejections and allowance of claims 1-9 is respectfully requested.

Respectfully submitted,

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